REMARKS

Claims 1-3 have been rejected under 35 USC 102 for anticipation by Tuttle. Although the claims have been amended herein, none of the amendments were made in response to this rejection. Instead, they were made to add an arguably missing element (the layer of silicon which could be argued to be not included in the transceiver integrated circuit element although this would be a stretch) and to clarify the fact that the insulation layer and the RFID tag or smart card integrated circuit is integrated on the device using integrated circuit fabrication techniques to make it clear that the claimed device is not comprised of layers which are glued to each other with conductive epoxy as is the case with the Tuttle reference.

With regard to the "plastic laminated to glass" limitation added to claims 1-3, this limitation was disclosed in original claim 3. Limitations added to later claims can be supported by limitations that were in the originally filed claims.

The amendments made to claim 3 just improve the form of the claims and make it clear that the insulation and transceiver layers of the integrated circuit being claimed in each claim are formed by integrated circuit fabrication techiques. No layer is glued to any other layer as is the case with Tuttle where the capacitor is glued to the battery and the transceiver is glued to the capacitor. These steps must be done manually by a person or a robot and make it impossible to make the Tuttle tages as cheaply as a fully integrated tag as claimed in claims 1-3.

These amendments made to claims 1-3 were not necessary to distinguish the prior art because the claim already contained at least two limitations, which, when properly interpreted, distinguish the Tuttle reference.

The Two Limitations Already Present Before This Amendment Which Distinguish Claims 1 and 2 Over Tuttle And the Reasons Therefor

First, claims 1 and 2 all already contained the limitation requiring the thickness of the layer of silicon dioxide or silicon nitride to be selected such that little or no differential strain between the layer of oxide or nitride and the underlying substrate at any temperature in the normal temperature range of the integrated circuit. Claim 3 only contains the limitations regarding the thickness of the insuation layer being selected to minimize differential strain, but this single difference is enough to distinguish Tuttle alone.

Second, claims 1-3 all use the clause "integrated on said substrate" in describing the structure of the RFID tag or smart card transceiver. An amendment was made herein to make it clear the the transceiver is integrated in the silicon layer, but it is still integrated on the subtrate as the term was originally used because the silicon layer is integrated on the substrate on top of the insuation layer so both the insulation layer and the silicon layer are "integrated on the substrate".

To better understand why these original limitations distinguish the prior art reference, please consider the following rules of law. First, the Examiner raised the "inherent anticipation" issue when he stated on page 5 of the Office Action that "Inherently, the high Young's Modulus silicon nitride can be optimized between 400 to 10,000 angstroms such that little or no differential strain between the substrate wherein the layer occurs at any temperature in the normal operating temperature range of the integrated circuit."

It is important to recognize that **accidental, unappreciated results should not be regarded as anticipatory**. Mycogen Plant Sci. Inc. v Monsanto Co., 243 F.3d 1316, 58 USPQ2d 1030 (Fed. Cir. 2001) [an accidental or unwitting duplication of an invention

cannot constitute anticipation]; Tilghman v. Proctor, 102 U.S. 707, 711-712 (U.S. 1880) [results that were accidently or unwittingly produced do not anticipate future discoveries].

Here, the Tuttle reference teaches at Col. 12, line 66 to Col. 13, line 24, the inclusion of a lamination of a barrier layer such as silicon nitride on the plastic substrate so as to provide a "hermetic barrier to prevent water vapor and other contaminants from affecting (e.g., oxidizing) the battery and transceiver components. The thickness of the deposit is taught to be from 400 to 10,000 angstroms, a range which includes the typical thickness range of the invention. Tuttle goes on to teach that where thin deposits are desired, both sides of the substrate can be covered with a thin layer so that pin holes do not line up and allow moisture to get to the battery. With regard to the thickness of the layer, Tuttle teaches:

> *The thickness of the deposit and the manner of formation are design choices based on the selection of materials for the film and the deposit, as well as the system requirements for hermeticity over time.*

Significantly, there is no teaching that the thickness of the nitride layer should be selected in cooperation with the Young's Modulus of the material being deposited so as to minimize differential strain between the insulation layer and the substrate. There is also no teaching in Tuttle anywhere that differential strain is a problem which can lead to device failure. **Tuttle clearly was not thinking about setting the thickness of the nitride layer to minimize different strain and did not even recognize differential strain as a problem. There is no suggestion anywhere in Tuttle that the thickness of the nitride barrier layer should be set for anything other than establishing good hermeticity.** As such, if Tuttle's nitride barrier layer were to have a thickness that did minimize the differential strain, it would be

a pure accident. More importantly, one skilled in the art when reading Tuttle would not appreciate the differential strain problem nor realize that some thicknesses of the barrier layer (depending upon the Young's modulus of the material selected) would minimize the differential strain. Clearly, most thicknesses of the stated range such as from 400 to 900 angstroms and from 3000-10,000 angstroms would not solve and would probably aggravate the different strain problem since for nitride the range which usually works to minimize differential stain is from1000 to 2000 angstroms. Thus, a thickness of 10,000 or 5,000 angstroms of nitride on a plastic substrate would almost certainly create sufficient differential strain to cause damage to the integrated circuit or bow the substrate and possibly cause cracking of brittle structures thereon.

Tuttle clearly was not aware or did not teach the problem of differential strain between the nitride layer and the substrate causing bowing of the substrate. Tuttle did not teach the relationship between the thickness of the nitride layer, Young's modulus and the substrate material and its Young's modulus. As such, any anticipation of the claimed invention would be perfectly accidental. *Since those skilled in the art were not apprised of the problem by Tuttle or the relationship between thickness, Young's modulus and differential strain, such workers in the art would not have appreciated any particular thickess for a nitride layer that would minimize differential strain.* Further, workers in the art would not appreciate that not every thickness in the range cited by Tuttle would work to minimize differential strain and that the thickness would have to be selected based upon the temperature range of use, the material and thickness of the plastic substrate and the material and thickness of the insulation layer, and balance all these factors so as to achieve minimum differential strain.

In deciding the issue of anticipation, first the claims must be properly interpreted to

determine their meaning in light of the specification, the claim language itself and the prosecution history. Then the properly interpreted claim elements must be compared to the allegedly anticipating reference.

Here the original limitations in claims 1-3 regarding the thickness of the silicon dioxide or silicon nitride layers being such that little or no differential strain between the insulation layer and the substrate occurs must be interpreted in light of the following passages from the specification.

From the Summary of the Invention, page 4, line 11:

> Second, reliability is increased. This is because the IC is formed on the same substrate as the antenna and there is a special coating on the plastic substrate to prevent mismatches in the coefficients of thermal expansion that caused differential strain in the prior art. This differential strain occurred at high temperatures and led to failures of prior art tags used in high temperature applications such as inside ovens. As used in the claims, the phrase "little or no differential strain between the substrate and said layer occurs in the normal operating temperature range of said integrated circuit" means not enough difference in the strain between the strain in the substrate at a given temperature and the layer of oxide, nitride or other material coated over the substrate occurs to cause fractures or stress that cause immediate or eventual reliability problems or failure of the circuit.

From the Summary, page 4, line 29:

> In a first class of embodiments, a polyester, PVC or polyimide or other plastic substrate has formed thereon a layer of silicon nitride or silicon dioxide. Hereafter, this layer will be referred to as the nitride layer, but

this terminology is to be intepreted as meaning the layer is made of silicon nitride, silicon dioxide or any other material that can be formed in such a thickness and has appropriate properties to reduce or eliminate the thermal coefficient of expansion mismatch reliability problem that is found in high temperature applications. The nitride layer serves to reduce or eliminate the reliability problems cause by mismatches in the coefficient of thermal expansion between the plastic substrate and the material of the transceiver chip that is bonded to the plastic substrate or the wirebond itself. The key to eliminating the reliability problems at high temperatures is to avoid mismatches in the amount of strain that occurs at a given temperature between the plastic substrate on which the antenna is fabricated and the the material on which the transceiver is fabricated and which is bonded to or integrated on the antenna bearing substrate. The amount of strain that occurs in a material in thermal expansion is a function of its Young's Modulus, the temperature and its geometry, especially its thickness. The trick then is to establish the thickness of the nitride layer (or whatever other material is chosen) so as to establish a "strain" value which substantially matches within about 5-10% or, preferably, exactly the strain value of the underlying plastic substrate at the same temperature given the geometry and material of the substrate.

From the Detailed Description of the Invention, page 12, line 9:

The key to avoiding reliability problems caused by differential thermal expansion is to coat the plastic substrate with a layer of silicon nitride (hereafter nitride) or silicon dioxide (hereafter oxide) or other material at a predetermined thickness to get matching strain values

between the plastic substrate and the coating layer. The thickness of the nitride or oxide layer 12A and 12B in Figure 1 must be selected such that the "strain" (the amount of deformation under thermal stress) in the oxide or nitride layer substantially (within 5-10%) or exactly matches the corresponding strain of the substrate 10 at the temperature of the operating environment given the geometry and material of the plastic substrate. Also, the oxide or nitride must be applied to both sides of the plastic substrate ~~substate~~ to avoid bowing the substrate at temperature.

Thus, the key to eliminating the reliability problems at high temperatures is to avoid differential strain which is so large as to cause fracturing, failure of the circuit electrically or mechanically or other reliability problems. The key to this is to avoid large mismatches in the amount of strain that occurs between the plastic substrate on which the antenna is fabricated and the the material on which the transceiver is fabricated and which is bonded to or integrated on the antenna bearing substrate at temperatures within the anticipated operating temperature range. This is the meaning of the phrase "reduce differential strain at anticipated operating temperatures so as to eliminate or reduce reliability problems".

The amount of strain that occurs in a material in thermal expansion is a function of its Young's Modulus, the temperature and its geometry, especially its thickness. The trick then is to establish the thickness of the nitride layer (or whatever other material is chosen) so as to establish a "strain" value which substantially matches within about 5-10% or, preferably, exactly the strain value of the underlying plastic substrate at

the same temperature given the geometry and material of the substrate. Nitride is a good choice for layers 12A and 12B because it has a high Young's Modulus so a thin layer, usually about 1000-2000 angstroms will cause the strain match desired at most operating temperatures experienced by RFID tags. Step 16 represents the process of depositing the right amount of nitride or oxide (or some other material) to achieve the strain match described above. This must be accomplished by a low temperature step with a maximum temperature below the melting point of the substrate 10. The nitride or oxide layers 12A and 12B can be sputtered on or deposited by a physical vapor deposition (PVD) or plasma enhanced chemical vapor deposition process (PECVD), all of which are known in the art and which may be performed at temperatures below 100 degrees C.

Low temperature processing steps to deposit PECVD silicon dioxide, nitride, gate oxides, amorphous silicon and aluminum on a PET substrate while limiting temperatures to less than 100 degrees C are disclosed U.S. patents 5,817,550 and 5,346,850, both assigned to the University of California, and in a paper by scientists at Lawrence Livermore National Labs, Theiss et al., *Polysilicon Thin Film Transistors Fabricated at 100 degrees C on a Flexible Plastic Substrate,* International Electron Devices Meeting Technical Digest, Page 257-260, 1998 the teachings of all of which are hereby incorporated by reference. IBM owns U.S. patent 5,796,121, the teachings of which are hereby incorporated by reference. This patent teaches methods and materials suitable to build a thin film transistor structure suitable for a flat panel

> display on inexpensive, clear plastic substrates such as Lexan® (polycarbonate). This IBM patent also teaches methods and materials to build multilayer TFT structures which will not delaminate, and an "upside down" TFT structure.

Clearly, these passages support integrating a nitride or oxide layer onto the substrate with a thickness which is selected to cause very little (within 5 to 10%) in the strain in the substrate insulation layer and the substrate. Clearly, this insulation layer is integrated onto the substrate using low-temperature, thin-film integrated circuit fabrication techniques.

Tuttle does not teach choosing a thickness for his barrier layer which is selected to minimize differential strain. With regard to the lack of teaching in Tuttle of selecting a thickness for the barrier layer to accomplish minimal differential strain consider the following rule of law. Where a reference makes no suggestion of any kind about its structural suitability for the claimed use, despite not explicitly describing anything inconsistent with that use, such a negative pregnant is not enough to show anticipation. Rowe v. Dror, 112 F.3d 473, 42 USPQ2d 1550, 1555 (Fed. Cir. 1997). Here, it seems that Tuttle does make an explicit teaching that would be inconsistent with selecting a thickness for the hermeticity barrier which minimizes differential strain in allowing the barrier to be up to 10,000 angstroms thick. This almost certainly would lead to massively mismatched strain values and cause severe bowing of the substrate and damage to other brittle structures on it at higher temperatures.

For anticipation to exist, a single reference must disclose each and every element of the claim with sufficient clarity to prove its existence in the prior art. Although this requirement presupposes the knowledge of those

skill d in the art, this presum d kn wl dge does n t grant a license to read into the prior art reference teachings which are n t ther . For example, an expert's conclusory testimony, unsupported by any documentary evidence, cannot supplant the requirement in law of anticipatory disclosure in the reference itself. Motorola, Inc. v. Interdigital Tech. Corp., 121 F.3d 1461, 43 USPQ2d 1481 (Fed. Cir. 1997).

Here, the Examiner has read teachings into Tuttle that are not there. Tuttle does not teach selecting a thickness for the barrier layer based upon its Young's modulus and the thickness and material and Young's modulus of the substrate so as to minimize differential strain between the substrate and the barrier layer.

Further, Tuttle does not teach integrating the integrated circuit transceiver of the RFID tag onto the substrate. The term "integrated" as used in the original claims, before this amendment meant using thin film integrated circuit processing techniques that were compatible with the preexisting structures so as to not destroy them. This process formed the integrated circuit *in situ* on the substrate in a layer of silicon which could be amorphous and which was deposited on the substrate and resulted in a different structure than Tuttle teaches. Tuttle teaches gluing the IC on the top of the capacitor using conductive epoxy. This is not an integrated structure. In an integrated structure, the layers are formed one on top of another and not glued to each other as in Tuttle. This creates a more reliable structure which is much cheaper to build.

SUPPORTFORNEWAMENDMENTS

With regard to support for other amendments regarding integrating structures onto the device using low-temperature, thin-film IC fabrication techniques, other passages from the specificaiton support using these techniques to form the layer of silicon, other insulation layers and the transceiver, processor and memory of the RFID tag or smart card which are also integrated on the device. If the Examiner is not able to find these passages in the specification, the undersigned will be happy to point out specific citations.

One such specific citation is from page 14, line 9 where the following paragraphs start:

> The upside down TFT structure of Figure 2 of the IBM patent is built in the following manner and may be adapted for use in the RFID tag or smart card applications if modified according to the teachings herein to add an antenna and suitable leader lines above the Hard Coat and prior to beginning construction of the TFT device. Gate metal from the group Cr, Ta, Mo, W and Cu and alloys thereof are next applied over the Hard Coat and patterned with Cr preferred. Next, three layers are applied in a reactor. First, a layer of gate dielectric, preferably amorphous silicon nitride is deposited at about 125 °C by the SiNitride PECVD process. Next, a layer of semiconductor for the channel is deposited at 125 °C by the a-Si:H PECVD process to form a layer of hydrogenated amorphous silicon (a-Si:H). Next, a layer of amorphous SiNitride is deposited by the same PECVD process used to deposit the gate dielectric. The amorphous SiNitride is then photolithographically patterned and etched to expose the semiconductor layer outside the island and a layer of phosphorous doped

N-type a-SiH silicon is deposited by PECVD. Alternatively, a low work function metal such as magnesium or yttrium may be used. A layer of metal such as Al, Cr or Ta is then deposited by evaporation or sputtering over the N-type a-SiH silicon layer. These last two conductive layers are then patterned photolithographically to form the desired interconnects. The finished structure can then be passivated. The structure for this upside down transistor can also be used as an alternative embodiment for the process used to build the structure shown in Figure 3 herein if the leader lines 92 and 94 are formed first on the Hard Coat followed by formation of antenna 88 in Figure 3 herein, and if the vias at 108 and 110 are formed through the IBM transistor insulation layer 58 in Figure 2 of the IBM patent. The same can be said for the structures of Figures 3 and 4 of the IBM patent.

The PECVD process IBM taught to deposit the dielectric layers is as follows. A PECVD process to deposit dielectric layers 58, 62, 78, 82, 100 and 104 in Figures 2,3 and 4 of the IBM patent is the following SiNitride process. The dielectric may be an amorphous Si, N, H alloy. The preferred process is to place the plastic substrate containing the patterned gate layer in a reactor at a temperature of 125 °C. in a gas mixture at a pressure in the range 0.1 to 1 Torr, the optimum pressure being 0.6 Torr. The gas mixture contains helium, nitrogen, ammonia and silane and the total gas flow is between about 500-2000 sccm with the optimum being about 875 sccm. For He/silane the flow ratio is between about 20/1 to 100/1, preferably about 60/1; for nitrogen/silane it is between about 15/1 to 25/1, preferably about 20/1; and for

ammonia/silane it is between about 1.2/1 to 2/1, preferably about 1.5/1. The preferred RF Power/area is about 0.05 Watts/cm^2, and may be in the range 0.03 to 0.1 Watts/cm.^{2}. Aluminum gate capacitor structures (here Al/SiNitride/Al) having a SiNitride dielectric film 2,670 Angstroms thick were made using this process. These capacitors exhibited a breakdown field of 6.4 MV/cm, and

leakage current at 1.1 MV/cm field of 6 x 10^{-9} Amps/cm^2. FIG. 5 shows the leakage current, curve 120, and the current breakdown, curve 122, at 6.4 MV/cm for these capacitors. These data show that this low temperature PECVD process is capable of depositing SiNitride having dielectric characteristics equivalent to those made by higher temperature PECVD processes utilizing different gas mixtures and other process parameters.

A PECVD process to deposit the a-Si:H channel layers 60, 80 and 102 in Figures 2, 3 and 4 of the IBM patent is as follows. The preferred process is to place the plastic substrate in a reactor at a temperature of 125 °C. and in a gas mixture at a pressure in the range 0.5 to 1.5 Torr, the optimum pressure being 1.0 Torr. The gas mixture contains He, hydrogen, and silane and the total gas flow is in the range of about 300-500 sccm, preferably about 350 sccm. For He/silane, the flow ratio is between about 10/1 to 50/1, preferably 20/1 and for hydrogen/silane it is between about 3/1 to 8/1, preferably 7/1. The preferred RF Power/area is about 0.03 Watts/cm^2 and may be in the range 0.02 to 0.05 Watts/cm^2. The resulting a-Si:H layers exhibit an optical gap of 1.85 eV, a refractive index of 3.86

and a hydrogen content of 20% with only monohydride bonding as characterized by infrared absorption spectroscopy and exhibit a ratio of photo/dark conductivity consistently >100,000. Both of these measurements are unchanged with several months time. FIG. 6 shows the ratio of photo/dark conductivity plotted vs. hydrogen/silane ratio. The photoconductivity was measured with a light fluence of about 0.1 Watts/cm.sup.2. The dark conductivity was measured inside a light tight metal box. The data points labelled 1 identify the preferred Hydrogen/Silane ratio. The dashed line labelled 132 shows the resulting ratio of photo/dark conductivity with no He used (i.e., only hydrogen). The data points labelled 134 illustrate the resulting ratio of photo/dark conductivity with no hydrogen (only He) used. These data show that this novel low temperature PECVD process is capable of depositing a-Si:H layers having semiconducting characteristics equivalent to those made by higher temperature PE CVD processes utilizing different gas mixtures and other process parameters.

The IBM patent teaches a low temperature way of forming a high quality gate dielectric characterized by leakage current density of less than about 1×10^{-8} amps/cm^2 and breakdown electric field of greater than 5 MV/cm and deposited at temperature of less than the glass transition temperature. Any other processing step that can form a layer of dielectric of this quality at a temperature below the glass transition temperature of the plastic substrate will also work for this step.

The IBM patent teaches ways of deposition of an amorphous

siicon layer having mid-gap defect densities of the order of $10^{16}/cm^3$ or less deposited at a temperature glass transition temperature of the plastic substrate. Any other process that can deposit a silicon layer of this quality at a temperature glass transition temperature of the plastic substrate will also work.

Olin Corporation owns a patent 4,877,641, the teachings of which are hereby incorporated by reference which teaches a low temperature way of depositing silicon nitride-type or silicon dioxide-type films on a substrate using temperatures from about 100° C to about 350° C. This process can be used as an alternative step to form the needed oxide and nitride layers in the IC being integrated onto a large plastic or glass substrate in place of the steps described elsewhere herein in alternative embodiments so long as the temperature of the deposition is not above the glass transition temperature of whatever plastic substrate is selected. This process involves introducing di-tert-butysilane and at least one other reactant gas into a CVD reaction zone containing the substrate on which the either a nitride or oxide film is to be formed, and maintaining the temperature of the zone and the substrate between 100° C to about 350° C and below the glass transition point of the substrate and maintaining the pressure in the zone from about 0.1 to 5 Torr. Then passing the gas mixture into contact with the substrate while exciting the gas mixture with a plasma for a period of time sufficient to form a silicon nitride-type or silicon dioxide-type film on the substrate with the plasma being excited by RF power at about 10 to 500 watts.

Another alternative embodiment of the processes described herein to form thin film transistors is to use flat panel display semiconductor processing equipment to practice a low temperature process of forming thin film transistors in amorphous silicon using DC reactive magnetron sputtering. This process is described in a paper by McCormick et al., *Low Temperature Fabrication of Amorphous Silicon Thin Film Transistors By DC Reactive Magnetron Sputtering*, J. Vac. Sci. Technol. A 15(5) Sept./Oct.1997, pp. 27702776 (May 1997), which is hereby incorporated by reference. This paper teaches deposition steps to deposit hydrogenated amorphous silicon and hydrogenated amorphous silicon nitride films using DC reactive sputtering at 125 and 230° C substrate temperatures. Metal-insulator-silicon transistors fabricated with this method on c-Si show electrical leakage of less than 5×10^{-8} A/cm^2 at 3 MV/cm field, flat band voltage magnitude of less than 1 volt, and hysteresis of less than 2 volts. Multiple inverted thin film transistors can be fabricated by this method on plastic substrates. Thin film transistors deposited at 125° C have field effect mobility of 0.3 cm^2/V.second and an I_{on}/I_{off} ratio of 5×10^5, and a threshold ratio of 3 volts.

The illustration in the figures of the preferred processes to be described next assumes only one transistor is being built, but those skilled in the art will appreciate that the following process steps apply equally to simultaneously building all the transistors needed to make an RFID transceiver by suitable fabrication of the masks. The following process is to be carried out simultaneously on large plastic substrates that can be

processed by flat panel semiconductor processing machines to build thousands or even millions of RFID tag transceivers simultaneously thereby lowering the per unit cost.

Step 20 represents the process of depositing a layer of amorphous silicon semiconductor 18 having a thickness of from 10-500 nanometers. The silicon can be sputtered on or deposited by PECVD at a temperature of about 100 degrees C. Transistors can be built in amorphous silicon, but they are not high speed transistors because mobilities, carrier lifetimes and other properties of amorphous silicon are not conducive to constructing high speed transistors. Fortunately, RFID tags do not need to be fast for most applications, so there is no need to improve the properties of the silicon. However, where higher performance transistors are desired, the silicon may be cyrstallized to polycrystalline or microcrystalline form by pulse annealing it with an XeCl excimer laser having a 308 nm wavelength. Typically, pulse durations of 30 nsec or less full width at half maximum per pulse are used with an energy density of 30-600 mJ/cm^2 per pulse, typically around 150 mJ/cm^2. This optional crystallization step is step 22 in Figure 2. Irradiating the silicon layer 18 with one or more pulses will partially or completely crystallize the silicon film producing a fully or partially crystalline channel poly-Si (hereafter poly) TFT. The TFT device constructed in this layer of poly will have higher ON currents, higher mobilities and lower threshold voltages than TFTs with an amorphous silicon channel.

Step 24 represents the process of depositing a layer of oxide

which will become the gate oxide 26. This layer is typically 20-500 nm thick and is deposited by PECVD at about 100 degrees C (sputtered oxide has not yet been shown to be of high enough quality for gate oxide). In alternative embodiments, the gate oxide 26 may also be nitride or a combination of nitride and oxide.

Next, a layer of gate metal such as aluminum that will become gate 28 is deposited, as symbolized by step 30. The gate metal layer is typically from 50-1000 nm thick, and is deposited by any suitable deposition technique such as PVD, CVD, evaporation or sputtering. Other metals or alloys such as Cu, Ni, Ti, Mo, Cr, Ta, W, Ti-Si, Ti-Al, Al-Si and Al-Cu can also be used. Also, doped silicon and silicides (silicon alloyed with a refractory metal) may also be used for the gate 28.

Step 32 represents the photolithographic definition of the thin film "island" containing the gate and gate oxide. This is done by conventional photolithography as modified for the plastic substrate. A typical example of such a process is as follows and will be referred to in the claims as "photolithographically etching" although this phrase is intended to cover all combinations of wet or dry type etching processes that are compatible with the plastic substrate chosen or at least which will not attack the coating that covers the plastic substrate and which will etch down through the layers above the semiconductor layer by one or more etching steps to leave the portions of the semiconductor layer exposed where source and drain doping is to occur:

1) bake the substrate containing the metal and gate oxide layers at 90 degrees C for 2 to 10 minutes;

2) spin on 1.4 micrometers of photoresist (a wide range of thicknesses from 0.5 to 2.5 micrometers is acceptable for this step);

3) prebake the photoresist coated substrate at 90 degrees C for 2 minutes;

4) expose the TFT gate pattern on the photoresist using a mask aligner;

5) develop the pattern using standard resist developer; and

6) postbake the substrate at 90 degrees C for 5 to 60 minutes;

7) the gate pattern is defined using standard wet chemical and/or plasma etching techniques. An example of how to do this follows. The exposed Al film is etched by immersion in Al-Type II etch manufactured by Ashland Chemical, for 5 minutes or until etching is complete, leaving an area of metal film as shown at 28 in Figure 1. This is followed by a deionized water rinse. The etching time will vary with the thickness of the gate film and the etch bath temperature which should be between 25 to 60 degrees C. Other wet chemical or dry chemical etches may also be substituted. Next, the sections of the gate oxide layer exposed by the metal etch are removed by immersion for 40 seconds in a well known etchant for etching oxide over semiconductor or contact metal, such as KTI Pad Etch I manufactured by Ashland Chemical. This leaves an area of gate oxide as shown at 26 in Figure 1. The etching time will vary with oxide thickness. Other wet or dry chemical etches may be substituted for this step. Finally, the remaining photoresist is removed using standard solvent and/or photoresist chemicals, followed by a rinse step.

This "photolithographic etching" process forms the "gate island"

which in the claims means the islands comprised of the gate 28 and gate-channel insulator 26 in Figure 1 or the or gate 126 and insulator 124 in Figure 3 or gate 178, insulator 176, floating gate 170 and insulator 168 in the EEPROM cell of Figure 8 and the corresponding structures in Figure 10. The above defined photolithographic etching process can be modified for making the EEPROM cell gate islands by addition of additional metal etch and insulation layer etch steps to define the floating gate and the insulator between the floating gate and the channel region.

Dry etches can be easily made anisotropic, so they are preferred if density of the ICs on the substrate is to be accomplished to lower the cost per unit since wet etches are more difficult to make anisotropic. However, where ICs for RFID tags are being made, the antenna size usually establishes the minimum size for the substrate so packing the ICs together more on the large substrate may not be needed, especially if it reduces yield.

Step 34 represents the process of crystallizing and doping the source and drain regions marked S and D in layer 18 of Figure 1. This is done using Gas Immersion Laser Doping (GILD) as described by P.G. Carey et al., IEEE Electron Devices Lett., Vol. EDL-7, No. 7, pp. 440-442 (1986). An example in this class of processes is as follows:

1) the thus processed plastic substrate is exposed to oxide etchant vapor such as HF vapor for several seconds, typically from 2-30 seconds to remove any native oxide from the exposed silicon layer 18;

2) the thus processed plastic substrate is then placed in a gas cell evacuated to a base pressure on the order of 3 mTorr and subsequently

filled to about 300 Torr with a dopant gas, for the GILD process. Typical gases are PF_5, BF_3, B_2H_6, PH_3, AsH_3 and AsF_5. Other base and dopant gas pressures may also be used. This creates a dopant layer on top of the silicon.

3) the resulting dopant film and the underlying silicon is then irradiated with several (2 to 1000) of laser energy at several laser fluences, increasing in steps from about 135 mJ/cm^2 to about 270 mJ/cm^2 for a time duration of from10 to 150 ns/pulse. The range of laser fluences will vary depending upon the exact layer thicknesses of the dopant and the underlying silcion and dopant materials selected. The ultimate range of laser fluences could be as wide as 30-600 mJ/cm^2. This laser heating locally remelts the silicon again and drives the doping materials into the poly to created doped source and drain regions. This Excimer Laser Annealing (ELA) step will result in two different device structures depending upon whether optional step 22 in Figure 2 was or was not performed. If step 22, was not performed, then step 34 results in doped polysilicon (poly) source and drain regions S and D in Figure 1 on either side of an undoped amorphous silicon channel region C. If optional step 22 was performed, then step 34 results in doped poly source and drain regions S and D on either side of an undoped poly channel region C. Other alternative methods for providing the doping may also be used such as predeposited dopant film followed by excimer laser annealing. To dope the source and drain regions P+, a layer of boron hydride should be deposited followed by ELA. To dope the source and drain regions N+, a

layer of phosphorous bearing compound should be deposited followed by ELA. Ion implantation followed by ELA could also be used as could low temperature CVD to do the doping.

Step 36 represents the process of photolithographically defining the "thin film transistor island" or TFT island. What this means is photolithography and etching is performed in the manner described previously so as to define the lateral extents at 38 and 40 in Figure 1 of the source and drain regions to isolate each MOS transistor from its neighboring devices. It means the same thing at the locations of any EEPROM or ROM cells being formed simultaneously on the same substrate. This prevents one transistors source and drain from being inadvertantly connected to the source or drain of neighboring devices. The photolithography is performed so as to not exceed the melting point of the plastic substrate during baking of the photoresist, and wet or dry etchants capable of etching poly are used to etch through the poly layer 18 down to the nitride layer 12B.

Step 42 represents the process of depositing an insulating layer such as the oxide shown at 44 to isolate the thin film transistor island from surrounding structures. Via holes are etched through this layer in step 48 to allow contacts to the source and drain layers to be formed. The insulation layer deposition step can be by the same process as used for step 24.

Step 50 represents the step of depositing a layer of "contact metallization....

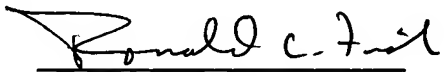
These low-temperature, thin-film integrated circuit processing techniques to form the

transceiver of the RFID tag or smart card of the device leave a distinct structure which is different than the Tuttle structure. For example, electrical contact in the Tuttle structure between the integrated circuit and the top place of the capacitor is taught at Col. 9, lines 39 to 42 to be made by conductive epoxy. This epoxy supplies both electrical contact and physical support for the IC. In contrast, in the claimed invention, support is intrinsically formed by the integrated circuit processes that deposit the various layers on each other, and electrical contact is supplied by via holes and metallization patterns. Thus, most if not all of the layers of the claimed device are formed as part of the integrated circuit processing process and no manual or robotic placement of capacitor on battery and IC on capacitor with glue dots is required. This means the device of the claims will be much cheaper to build and probably will be more reliable.

A new claim 4 has been added to claim the EEPROM built on a plastic substrate of Figure 8.

Respectfully submitted,

Dated: October 15, 2003



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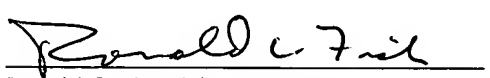

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